PHSA –VIIIA

Full marks 50 Time 2 hrs

*Answer any **one** question*

1.

(a) Draw the circuit diagram of a series regulated power supply from a given unregulated power supply using two transistors and a zener diode. (10)

(b) Using the following data determine the values of the resistances used in the above circuit for output regulated voltage = 12 Volt for current range (0 – 100 mA).
Output voltage of unregulated power supply $V_{in(min)}$ = 10 Volt to $V_{in(max)}$ = 15 Volt
β for pass transistor = 200
β for error amplifier = 100
Breakdown voltage of Zener diode = 5.6 Volt at I_Z =10 mA (10)

(c) What do you mean by load regulation characteristics of the above circuit?
Give a schematic diagram of a load regulation characteristic.
Using the above schematic diagram, how can you calculate the percentage regulation?
(3 + 4 + 3)

(d) Using the following data for line regulation, draw the line regulation curve for the above circuit for load current I_L = 10 mA in a mm division graph paper.

V_{in} (Volt)	V_{out} (Volt)
10	9.3
11	10.5
12	11.0
13	11.6
14	11.8
15	11.9

Calculate % regulation of the curve

(7 + 3)

(e) Draw the Bridge Rectifier circuit diagram with capacitor filter.
Why is the percentage regulation of the above Bridge Rectifier low for high output current with such filter?
Is percentage regulation of a bridge rectifier without filter more than that with filter? Explain the reason.
(4 + 3 + 3)

Or

Explain the working Principle of the series regulated power supply. (10)

2.

(a) Draw the circuit diagram for symmetrical astable multivibrator using two transistors (of almost equal values of h_{FE}) (5)

(b) Using the following circuit components design the circuit to produce a square wave of frequency 4.8 KHz

h_{FE} of the transistors used = 170

D.C. voltage source = 5 Volt

$I_{C(sat)}$ of each transistor = 5 mA

$V_{CE(sat)}$ = 0.1 Volt (5)

(c) Draw the schematic diagram of the square wave which is observed in an Oscilloscope. Indicate the "On Time" and "Off Time" in the diagram (3 + 2)

(d) How can you convert the above symmetrical astable multivibrator to asymmetrical one where "On Time" of a transistor is double the "Off Time".

(5)

(e) The square wave produced by the above symmetrical astable multivibrator circuit is observed through an oscilloscope with time/div = 0.1 ms. What will be the total number of divisions in time scale to accommodate 4 such complete cycles? (5)

(f) Explain the working principle of astable multivibrator.
Draw the nature of variation of V_{BE} of a transistor for a complete cycle. (10 + 5)

(g) Name two other types of mutivibrators with short description of each one. (10)

Or

Give the circuit diagram of an astable multivibrator using OPAMP. Write the expression for time period of the multivibrator. (5 + 5)

3.

(a) Draw the circuit diagram of a voltage amplifier using a transistor in common emitter mode with voltage divider bias. The emitter resistance of the transistor is short circuited by a suitable capacitor. (5)

(b) Design the above amplifier using the following data with lower and upper cut-off frequencies at 1 KHz and 300 KHz respectively and with mid band gain = 100
V_{CC} =12 Volt, I_C = 5 mA
Parameters of the transistor β = 150 and h_{ie} = 150

(10)

(c) The output voltage V_0 recorded with the variation of input voltage V_i at frequency f = 20 KHz. The corresponding data are given below.

V_i (Volt)	V_0 (Volt)
0.005	0.51
0.01	1.02
0.02	2.03
0.03	3.05
0.04	4.04
0.05	4.76
0.06	5.20
0.07	5.40

Draw the V_0 vs. V_i curve in a mm graph paper, hence indicate the linear region. Suggest a suitable input voltage for frequency response characteristic of amplifier.

(5 + 2)

(d) Draw a schematic diagram of frequency response curve and indicate (i) lower cut-off frequency, (ii) a mid-band frequency and (iii) upper cut-off frequency on that curve.

(2 + 3)

(e) What are the phase relationship between input and output signal at (i) lower cut-off frequency, (ii) mid-band frequency and (iii) upper cut-off frequency of a CE amplifier

(3)

(f) Explain the use of short circuit capacitor connected with emitter of the transistor.

(5)

(g) How can you reduce the gain of the amplifier from 100 to 75 without disturbing the D.C. bias.

(5)

(h) Draw the output characteristic of a transistor in CE mode.
Draw a load line for the transistor
What does the slope of the load line indicate?
Indicate Q point on the characteristics curve.

(4 + 2 + 2 + 2)

4.

(a) What are the properties of an ideal OPAMP that differ from a practical OPAMP?

(5)

(b) What is input offset voltage of an OPAMP? How input offset voltage is being nullified before starting the experiment?

(2 + 3)

(c) Draw the circuit diagram of an inverting amplifier using OPAMP. Mention the values of the resistances for gain -15 and -27.

(3 + 2)

(d) Design a Schmitt Trigger using an OPAMP, Power supply = ± 12 Volt and a Zener diode (V_Z = 5.6 Volt) with feedback ratio 1:11.
Calculate triggering voltage and hysteresis voltage for the circuit
Explain the working principle of the above Schmitt Trigger circuit.
How can you change the triggering voltage and hysteresis voltage?

(3 + 2 + 5 + 3 + 2)

(e) Draw the circuit diagram and design a differentiator circuit using OPAMP with operating frequencies less than 1 KHz.
Why a series resistance is connected with the capacitor in the above differentiator circuit?
How can be the value of capacitor determined from V_0 (output rms voltage)/V_i (Input rms voltage) vs. f (Frequency) curve of a differentiator?

(5 + 5 + 5)

(f) What are the voltages observed at the inverting and non-inverting terminals in the active and saturation region with positive input voltage? Explain your answer.

(5)

5.

(a) Draw the circuit diagram of a non-inverting amplifier using OPAMP. How the input offset voltage is being nullified before starting of the experiment?
Write down the expression of gain of the non-inverting amplifier and mention the notations used.
Following input and output data for a non-inverting amplifier experiment are recorded

V_{in} (Volt)	V_{out} (Volt)
-0.60	-11.80
-0.50	-11.50
-0.40	-9.25
-0.20	-4.20
0.00	0.00
0.20	4.32
0.40	9.31
0.50	11.45
0.60	11.20

Draw V_{out} vs. V_{in} curve in a mm graph paper and hence find the gain of the circuit. Can you predict the resistances used for the circuit?

(3 + 3 + 3 + 5 + 3 + 3)

(b) Draw the circuit diagram of a differential amplifier using OPAMP.
In a differential amplifier circuit the series resistances connected to the input terminals are 1 KΩ each and other resistances are 10 KΩ each. The voltages applied to the end of 1 KΩ resistances connected to inverting and non-inverting terminals are 0.20 volt and -0.20 volt respectively. Determine the expected output voltage and estimate the voltages at pin No. 2 (inverting terminal) and 3 (non inverting terminal) of OPAMP chip 741 (Assume the input offset is nullified before doing the experiment)

(3 + 3 + 4)

(c) Draw the circuit diagram of an integrator circuit using an OPAMP, where 100 KΩ register is connected across the capacitor used in the circuit. Mention the values of the resistances and capacitor when operating frequency of the integrator is above 10 KHz.
Draw the schematic diagram of V_i (input rms voltage)/V_{out} (output rms voltage) vs. f (Frequency) curve. How can you estimate the face value of the capacitor used for the experiment from the curve?
What is the utility of the high resistance connected parallel to the capacitor?

(3 + 3 + 3 + 3 + 3)

(d) What are the properties of an ideal OPAMP that differ from a practical OPAMP?

(5)

6.

(a) Draw the circuit diagram of a lead-lag network used in a Wien Bridge Oscillator. Draw (i) The phase shift vs. Frequency curve (ii) V_{out} /V_{in} vs. Frequency curve for the lead-lag network
Explain the nature of variation of the above curves.

(3 + [3 + 3] + [3 + 3])

(b) Draw the circuit diagram and design a Wien Bridge Oscillator for frequency = 7.2 KHz
Explain the importance of lead-lag network in the Wien Bridge Oscillator.
Comment on the values of resistances used in the circuits other than lead-lag network.
How does the output voltage vary with variation of Resistance R_3 of the Wien Bridge circuit? Explain the utility of R_3.

([5 + 5] + 5 + 5 +[2 + 3])

(c) Name two oscillators other than Wien Bridge Oscillator.
Draw the circuit diagram of an Oscillator you have mentioned above.
Give the expression for the frequency of the oscillator.

(2 + 5 + 3)

7.

(a) Draw the circuit diagram of a temperature controller using OPAMP, thermistor, transistor and relay.

(10)

(b) Design the above circuit with the following data
D.C. Power supply = ± 12
Variation of thermistor voltage for a given series resistance are from 93.4 mV to 27.8 mV with the variation of temperature 30^o C to 85^o C.
Resistance of the relay coil = 100 Ω at (30^o C)
β of the transistor = 150

(15)

(c) Variation of voltage across the thermistor with respect to the temperature are as follows

T (^{o}C)	V(mV)
30	93.4
37	81.5
42	71.8
47	64.3
51	56.2
56	51.8
61	45.9
65	42.8
75	36.1
79	32.2
85	27.8

Draw the calibration curve using the above data in a mm graph paper.

To maintain the water bath at 60°C, calculate the reference voltage for the comparator of the above circuit.

(5 + 5)

(d) At the almost steady temperature of the water bath (at 60°C ± 2°C) what are the voltages at

i. Output terminal of amplifier OPAMP

ii. Output terminal of comparator OPAMP

iii. Collector of the transistor

(5 + 5 +5)

8.

(a) Draw the circuit diagram of S-R Flip Flop using NAND/NOR Gate **without enable/disable terminal** and write down sequential table and Truth Table of the circuit.

(3+3)

(b) Draw the circuit diagram of S-R Flip Flop using NAND/NOR Gate **with enable/disable terminal** and write down sequential table and Truth Table of the circuit.

(3+3)

(c) Draw the circuit diagram of J-K Flip Flop using NAND/NOR Gate **without enable/disable terminal** and write down sequential table and Truth Table of the circuit.

(3+3)

(d) Draw the circuit diagram of J-K Flip Flop using NAND/NOR Gate **with enable/disable terminal** and write down sequential table and Truth Table of the circuit.

(3+3)

(e) What are the differences between an S-R Filp Flop and a J-K Flip Flop in terms of connection and behaviour?

(3)

(f) An S-R Flip Flop is constructed using 2-input NAND gates only. Initially, power is switched off and both the inputs are grounded. After tuning on the power source which output (Q or Q′) will be in 'one' state? Explain your answer.

(3)

(g) Define 4:1 Multiplexture. Draw a circuit diagram of a 4:1 Multiplexure and explain its working principle with the help of truth table.

(1 + 3 + 3)

(h) Explain working principle of a 1:4 Demultiplexure with help of diagram and truth table.

(6)

(i) List the ICs you have used to construct the above circuit. Draw the Pin Configuration of each IC.

(2 + 5)