2024

PHYSICS — HONOURS

Paper : CC-13

(Digital Systems and Applications)

Full Marks : 50

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

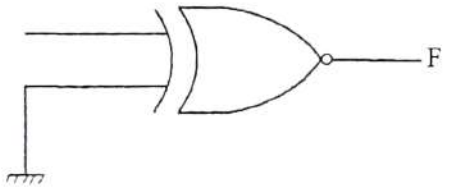
Answer ***question no.*** **1** and ***any four*** from the rest.

1. Answer ***any five*** questions : 2×5

(a) Define EPROM.

(b) Prove that $Y = (\bar{A} + B)(A + B + D)\bar{D} = B\bar{D}$.

(c) Determine the output expression :



(d) How can we use an 8 : 1 Mux as 3 input EX-OR gate?

(e) Mention the differences between synchronous and asynchronous counters.

(f) Why is a Flip-Flop called 1-bit memory?

(g) Draw the circuit diagram of OR gate using TTL logic and write down its truth table.

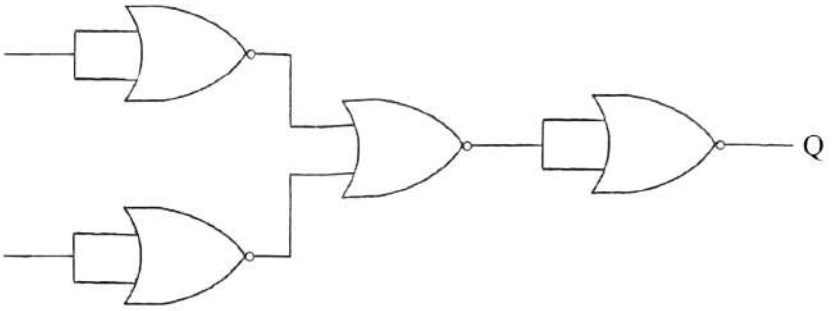
2. (a) Convert the hexadecimal number A6E.CD into octal number.

(b) Using 2's complement method, find Y – X where X = 100101 and Y = 11100.

(c) Implement the given Boolean expression $Y = AB + \bar{A}\bar{B}$ using NOR gates only. 3+3+4

3. (a) Using Karnaugh map, simplify the Boolean function $F(A, B, C, D) = \sum m(0, 2, 4, 7, 8, 10, 12, 13)$.

   (b) Which gate can be realised by the following circuit?



   (c) What is a half adder? Draw a full adder circuit using two half adders. From it, obtain the expressions for sum and carry of a full adder. [3+2+(1+2+2)]

4. (a) Draw the block diagram of a 4-bit binary adder subtractor.

   (b) What do you mean by decimal-to-BCD encoder? Draw the logic diagram of a decimal-to-BCD encoder.

   (c) Design a combinational logic circuit using a suitable decoder and OR gates to implement the functions $F_1(A, B, C) = \sum m(2, 3, 6, 7)$ and $F_2 = \sum m(1, 2, 5, 7)$. 3+(2+2)+3

5. (a) Draw a clocked SR flip-flop using NAND gates only. Convert it into a JK flip-flop. Explain the operation of JK flip-flop with its truth table.

   (b) What is race around condition? How can it be avoided? [(2+2+2+2)+(1+1)]

6. (a) Draw a 4-bit serial-in-parallel-out shift register using JK flip-flops. Explain its operation for the input 1011.

   (b) How many flip-flops are required to make a MOD-32 binary counter?

   (c) Data from a satellite is received in serial form (1 bit after another). If this data is coming at a 5 MHz rate and if the clock frequency is 5 MHz, how long will it take to serially load a word in a 32-bit shift register? 5+3+2

7. (a) For an 8-bit D/A converter with a full scale output of 10 volt, calculate its resolution. How many comparators are required to design a 4-bit flash (parallel) type A/D converter?

   (b) Describe the differences between PLA and PAL logics.

   (c) For a 10-bit digital ramp ADC using 500 kHz clock, what is the maximum conversion time? [(3+3)+2+2]